CLAIMS

1. A memory module, comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface for receiving memory requests for access to at least one of the memory devices;

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices;

a switch for selectively coupling the link interface and the memory device interface; and

a direct memory access (DMA) engine coupled through the switch to the memory device interface, the DMA engine generating memory requests for access to at least one of the memory devices to perform DMA operations.

2. The memory module of claim 1 wherein the memory hub is an embedded system having the link interface, the memory device interface, the switch, and the DMA engine residing in a single device.

3. The memory module of claim 1 wherein the memory device interface comprises:

a memory controller coupled to the switch through a memory controller bus and further coupled to the memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to at least one of the memory devices to which the memory controller is coupled; and

a cache coupled to the memory controller for storing data provided to the memory devices or retrieved from the memory devices.

4. The memory module of claim 1 wherein the switch comprises a cross-bar switch.

5. The memory module of claim 1 wherein the plurality of memory devices is a bank of memory devices simultaneously accessed during a memory operation.

6. The memory module of claim 1 wherein the plurality of memory devices comprise synchronous dynamic random access memory devices.

7. The memory module of claim 1 wherein the DMA engine comprises:

an address register for storing a starting memory address for a DMA operation;

a target address location for storing a target address of a location to which data is to be moved in the DMA operation;

a count register for storing a count value indicative of the number of memory locations to be accessed in the DMA operation; and

a next register for storing a value representative of the completion of the DMA operation or representative of a memory address corresponding to a link list including a starting memory address, a count value and a next memory address to be loaded into the address register, the count register, and the next register.

8. A memory hub for a memory module having a plurality of memory devices, comprising:

a link interface for receiving memory requests for access at least one of the memory devices;

a memory device interface for coupling to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices;

a switch for selectively coupling the link interface and the memory device interface; and

a direct memory access (DMA) engine coupled through the switch to the memory device interface, the DMA engine generating memory requests for access to at least one of the memory devices to perform DMA operations.

9. The memory hub of claim 8 wherein the link interface, the memory device interface, the switch, and the DMA engine are embedded systems residing in a single device.

10. The memory hub of claim 8 wherein the memory device interface comprises:

a memory controller coupled to the switch through a memory controller bus and further coupled to the memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to at least one of the memory devices to which the memory controller is coupled; and

a cache coupled to the memory controller for storing data provided to the memory devices or retrieved from the memory devices.

11. The memory hub of claim 8 wherein the switch comprises a cross-bar switch.

12. The memory hub of claim 8 wherein the DMA engine comprises:

an address register for storing a starting memory address for a DMA operation;

a target address location for storing a target address of a location to which data is to be moved in the DMA operation;

a count register for storing a count value indicative of the number of memory locations to be accessed in the DMA operation; and

a next register for storing a value representative of the completion of the DMA operation or representative of a memory address corresponding to a link list including a starting memory address, a count value and a next memory address to be loaded into the address register, the count register, and the next register.

13. A memory system, comprising:

a memory bus on which memory requests are provided; and

at least one memory module coupled to the memory bus, the memory module having a plurality of memory devices and a memory hub, the memory hub comprising:

a link interface coupled to receive memory requests for access to at least one of the memory devices of the memory module on which the link interface is located;

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices;

a switch for selectively coupling the link interface and the memory device interface; and

a direct memory access (DMA) engine coupled through the switch to the memory device interface and the link interface, the DMA engine generating memory requests for access to at least one of the memory devices to perform DMA operations.

14. The memory system of claim 13 wherein the memory hub is an embedded system having the link interface, the memory device interface, the switch, and the DMA engine residing in a single device.

15. The memory system of claim 13 wherein the memory bus comprises a high-speed memory bus.

16. The memory system of claim 13 wherein the memory bus comprises a high-speed optical memory bus and wherein the link interface comprises an optical memory bus interface circuit for translating optical signals and electrical signals.

17. The memory system of claim 13 wherein a plurality of memory modules are included in the memory system and a first memory module of the plurality of memory modules is coupled to the memory bus and the remaining memory modules of the plurality are coupled in series with the first memory module.

18. The memory system of claim 13 wherein a plurality of memory modules are included in the memory system and each of the plurality of memory modules are coupled directly to the memory bus through a respective link interface.

19. The memory system of claim 13 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the switch through a memory controller bus and further coupled to the memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to at least one of the memory devices to which the memory controller is coupled; and

a cache coupled to the memory controller for storing data provided to the memory devices or retrieved from the memory devices.

20. The memory system of claim 13 wherein the switch of the memory hub comprises a cross-bar switch.

21. The memory system of claim 13 wherein the plurality of memory devices of a memory module represents a bank of memory devices simultaneously accessed during a memory operation.

22. The memory system of claim 13 wherein the plurality of memory devices of the memory modules comprise synchronous dynamic random access memory devices.

23. The memory system of claim 13 wherein the DMA engine of the memory hub comprises:

an address register for storing a starting memory address of a memory location in the memory system at which a DMA operation begins;

a target address location for storing a target address of a memory location in the memory system to which data is to be moved in the DMA operation;

a count register for storing a count value indicative of the number of memory locations to be accessed in the DMA operation; and

a next register for storing a value representative of the completion of the DMA operation or representative of a memory address corresponding to a link list including a starting memory address, a count value and a next memory address to be loaded into the address register, the count register, and the next register.

24. A computer system, comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU, the system controller having an input port and an output port;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller;

at least one memory module, the memory module comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface coupled to receive memory requests for access to at least one of the memory devices of the memory module on which the link interface is located;

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices;

a switch for selectively coupling the link interface and the memory device interface; and

a direct memory access (DMA) engine coupled through the switch to the memory device interface and the link interface, the DMA engine generating memory requests for access to at least one of the memory devices of the plurality of memory modules to perform DMA operations; and

a communications link coupled between the system controller and at least one of the plurality of memory modules for coupling memory requests and data between the system controller and the memory modules.

25. The computer system of claim 24 wherein the communications link comprises a high-speed memory bus.

26. The computer system of claim 24 wherein the memory hub is an embedded system having the link interface, the memory device interface, the switch, and the DMA engine residing in a single device.

27. The computer system claim 24 wherein the communications link comprises a high-speed optical memory bus and wherein the link interface of the memory hub comprises an optical memory bus interface circuit for translating optical signals and electrical signals.

28. The computer system of claim 24 wherein a plurality of memory modules are included in the computer system and a first memory module of the plurality of memory

modules is coupled to the communications link and the remaining memory modules of the plurality are coupled in series with the first memory module.

29. The computer system of claim 24 wherein a plurality of memory modules are included in the computer system and each of the plurality of memory modules are coupled directly to the memory bus through a respective link interface.

30. The computer system of claim 24 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the switch through a memory controller bus and further coupled to the memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to at least one of the memory devices to which the memory controller is coupled; and

a cache coupled to the memory controller for storing data provided to the memory devices or retrieved from the memory devices.

31. The computer system of claim 24 wherein the switch of the memory hub comprises a cross-bar switch.

32. The computer system of claim 24 wherein the plurality of memory devices of a memory module represents a bank of memory devices simultaneously accessed during a memory operation.

33. The computer system of claim 24 wherein the plurality of memory devices of the memory module comprise synchronous dynamic random access memory devices.

34. The computer system of claim 24 wherein the DMA engine of the memory hub comprises:

an address register for storing a starting memory address of a memory location in the memory system at which a DMA operation begins;

a target address location for storing a target address of a memory location in the memory system to which data is to be moved in the DMA operation;

a count register for storing a count value indicative of the number of memory locations to be accessed in the DMA operation; and

a next register for storing a value representative of the completion of the DMA operation or representative of a memory address corresponding to a link list including a starting memory address, a count value and a next memory address to be loaded into the address register, the count register, and the next register.

35. A method for executing memory operations in a computer system having a processor, a system controller coupled to the processor, and a system memory having at least one memory module coupled to the system controller through a memory bus, the method comprising:

writing direct memory access (DMA) information to a location in the system memory representing instructions for executing memory operations in the system memory without processor intervention;

obtaining control of the memory bus from the processor and system controller;

accessing the location in the system memory to which the DMA information is written; and

executing the memory operations represented by the instructions.

36. The method of claim 35, further comprising isolating the system memory during execution of the memory operations.

37. The method of claim 35 wherein writing DMA information comprises:

writing a starting memory address of a memory location in the system memory at which the memory operations begins;

writing a target address of a memory location in the system memory to which data is to be moved in the memory operations;

writing a count value indicative of the number of memory locations to be accessed in the memory operations; and

writing a next memory address value representative of the completion of the memory operations or representative of a memory address corresponding to a link list including a starting memory address, a count value and a next memory address value.

38. The method of claim 35 wherein the system memory comprises a plurality of memory modules and wherein executing the memory operations comprises accessing a memory location in a first of the plurality of memory modules to read data therefrom and accessing a memory location in a second of the plurality of memory modules to write the data.

39. A method for transferring data within a system memory included in a computer system having a processor, a system controller coupled to the processor, and a memory bus coupling the system controller to the system memory, the method comprising:

writing DMA instructions to a location in the system memory, the DMA instructions representing instructions for executing memory operations to transfer the data including memory addresses corresponding to first and second locations in the system memory;

obtaining control of the memory bus; and

without processor intervention, accessing the location in the system memory at which the DMA instructions are written, reading data from the first location in the system memory and writing the data to the second location in the system memory.

40. The method of claim 39 wherein obtaining control of the memory bus comprises isolating the system memory from the processor and system controller while transferring data within the system memory.

41. The method of claim 39 wherein writing DMA instructions comprises:

writing a starting memory address of a memory location in the system memory at which the transfer of data begins;

writing a target address of a memory location in the system memory to which the data is to be transferred;

writing a count value indicative of the number of memory locations to be accessed in transferring the data; and

writing a next memory address value representative of the completion of the data transfer or representative of a memory address corresponding to a link list including a starting memory address, a count value and a next memory address value.

42. The method of claim 39 wherein the system memory comprises a plurality of memory modules and wherein reading data from the first location in the system memory comprises accessing a memory location in a first of the plurality of memory modules to read data therefrom and writing the data to the second location in the system memory comprises accessing a memory location in a second of the plurality of memory modules to write the data.